Specification of FC3860A

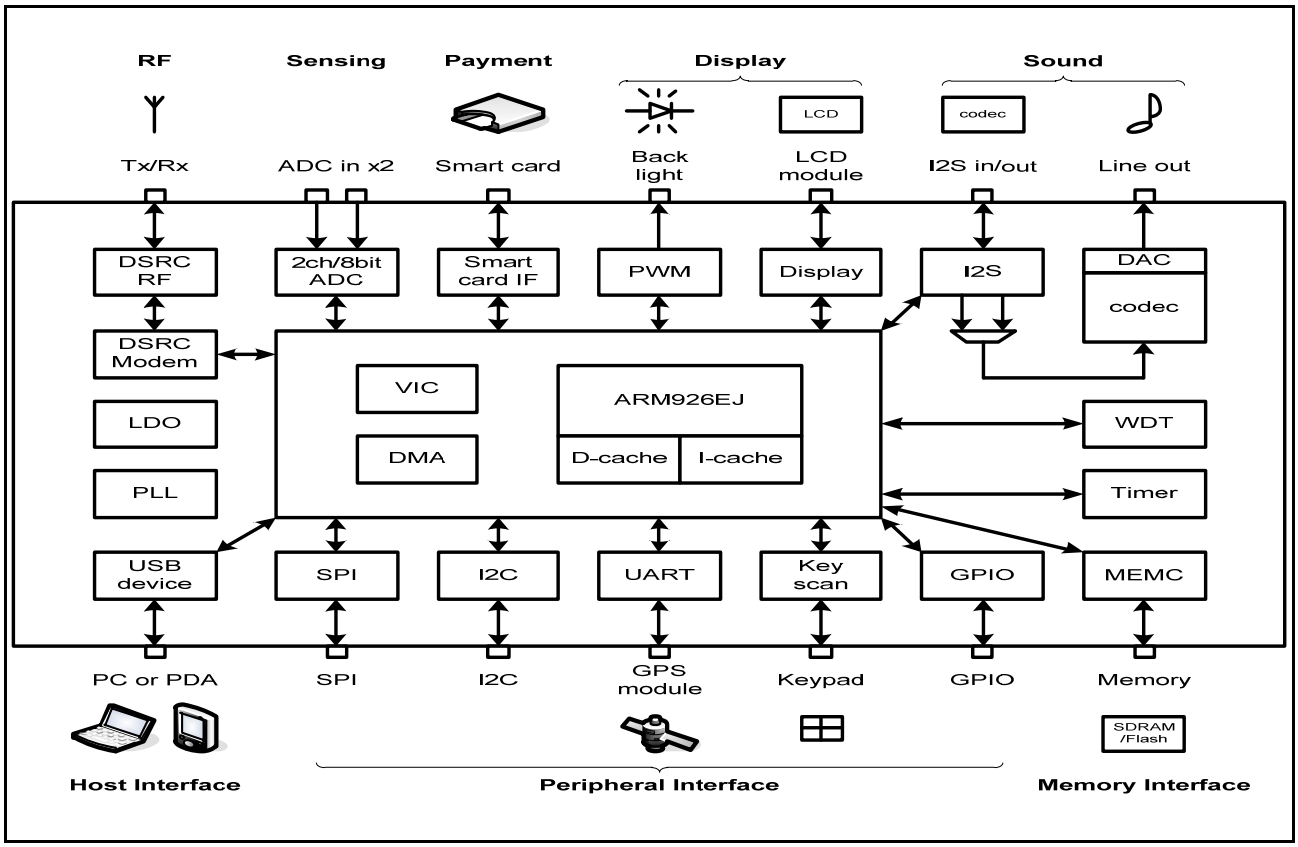
Single-chip 5.8GHz DSRC modem
Integrated with RF and MCU

Data Sheet
Brief ver.

1. Overview

1.1. Introduction

FC3860A is a single-chip SoC for electronic toll collection, in which 5.8GHz RF, DSRC modem, and MCU are integrated. The chips provide performance and functions which conform to the Korean DSRC standard, TTAS.KO-06.0025/R1.



[Figure 1 FC3860A block diagram]

Various peripherals like smart card interface, USB, DAC, ADC, LCD interface, keypad scanner, UART, SPI, IIC, IIS, etc are integrated.

Software development kit (SDK) that fully covers all the parts of the SoC is also provided. Users can easily develop their own DSRC applications through the well-defined APIs.

With its high-level of integration, small size, high performance, ease of use the FC3860A is the ideal choice for ETCS (Electronic Toll Collection System), ATIS (Advanced Traveler Information System), and other various DSRC applications.

1.2. Features

- RF
  - Frequency range: 5790MHz ~ 5840MHz
  - Automatic temperature calibration for output power and sensitivity using internal temperature sensor
  - Optimized for the lowest BOM
    - ✓ No external IF SAW filter
  - Operating Temperature
    - ✓ FC3860A: -40℃ ~ +105℃
  - Sensitivity: -85dBm with additional LNA
  - Output power: 8dBm with additional PA
  - Spurious emission: > 40dBc
  - ACLR: > 40dBc
  - Fast Rx/Tx switching time: < 18us
- DSRC
  - Compliance to Korea TTA
  - Manchester decoder with automatic synchronization function
  - Programmable TXD timing control
- Processor
  - ARM926EJ
    - ✓ CPU speed of up to 160MHz
    - ✓ 32kB/16kB instruction/data cache
  - Boot
    - ✓ NAND/NOR flash
- Built-in Analog Devices
  - 16 bit Audio DAC
  - 2-channel 8 bit ADC
  - Full on-chip LDO in RF block and high loading current LDO for DSRC/ARM
- Peripherals
  - Memory controller
    - ✓ SDRAM: 16/32-bit, up-to 512Mb
    - ✓ Asynchronous static memory: 8/16-bit, SRAM, NOR flash
    - ✓ Static memory features included
    - ✓ Two chips selects each for dynamic and static memory

- NAND flash controller
  - ✓ NAND flash, with ECC hardware acceleration for pages raging from 256 to 8192 bytes
- LCD module support
  - ✓ SPI and 4/8/16 bit parallel interface(8080-like interface and 6800-like interface)
  - ✓ PWM for back light control
- Smart card interface: ISO7816
  - ✓ Support asynchronous T0 and T1 transmission protocols
  - ✓ Support clock rate conversion factor F=372, with bit rate adjustment factors D=1,2,or 4
  - ✓ 8 character deep buffered TX and RX paths
  - ✓ Direct interrupts for TX and RX FIFO level monitoring
  - ✓ Hardware initiated card deactivation sequence on detection of card removal
  - ✓ Software initiated card deactivation sequence on transaction complete
- USB 1.1 FS device
  - ✓ Full-Speed(12MHz) support
  - ✓ Support control, interrupt, bulk and isochronous transfer
  - ✓ FIFOs are housed inside core for both data-out and data-in paths
  - ✓ Six bidirectional endpoints + Control endpoint0
- DMA
  - ✓ 8 DMA channels, Each channel can support a unidirectional transfer
  - ✓ 16 DMA requests
  - ✓ Single DMA and burst DMA request signals
  - ✓ Memory-to-memory, memory-to-peripheral, peripheral-to-memory and peripheral-to-peripheral
- Interrupt Controller
  - ✓ Support for 32 vectored IRQ interrupts
  - ✓ Fixed or programmable interrupt priority levels
  - ✓ IRQ and FIQ generation
  - ✓ Software interrupt generation
- Timers
  - ✓ Four 32/16-bit down counters with free-running, periodic and on-shot modes
  - ✓ Common clock with separate clock-enables for each timer gives flexible control of the timer intervals
- Watchdog Timer
  - ✓ 32-bit down counter with a programmable timeout interval
  - ✓ Separate watchdog clock with clock enable for flexible control of the timeout interval

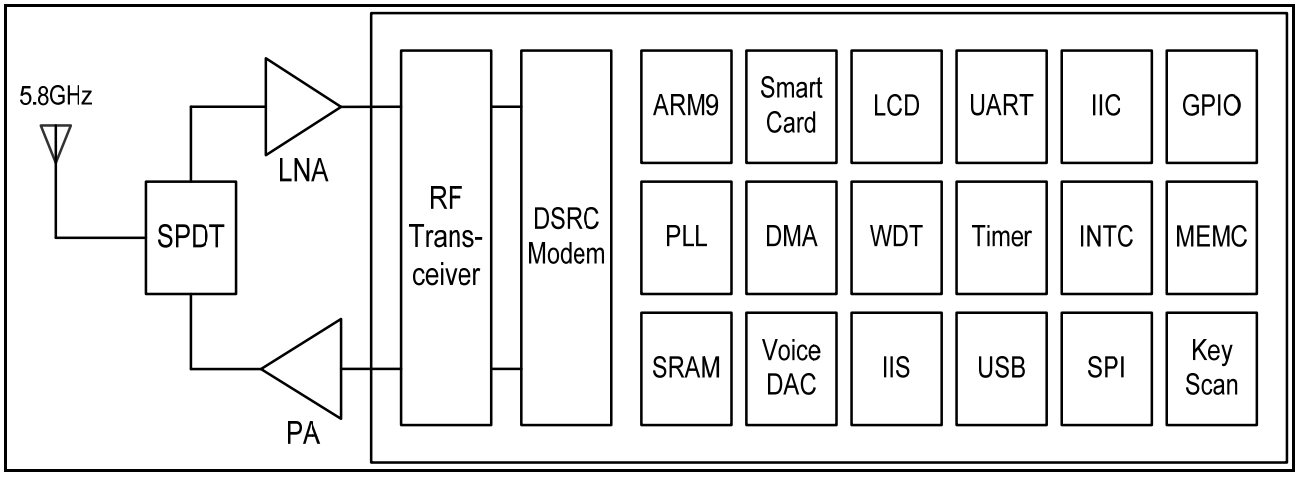
- Two I2C-bus interfaces
- Two SPI interfaces
  - ✓ Motorola SPI-compatible interface
  - ✓ Texas Instruments synchronous serial interface
  - ✓ National Semiconductor Micro-wire interface
- Three UART interfaces
  - ✓ Support for DMA
  - ✓ Separate 32x8 transmit and 32x12 receive FIFO
  - ✓ Programmable FIFO disabling for 1-byte depth
  - ✓ Programmable baud rate generator
  - ✓ False start bit detection
- I2S interface
  - ✓ The transmitter/receiver FIFO
  - ✓ Support for DMA
- GPIO
  - ✓ Five groups of GPIOs
  - ✓ Each group has eight individually programmable input/output pins, default to input at reset
  - ✓ Programmable interrupt generation capability, from a transition or a level condition
  - ✓ Bit masking in both read and write operations through address lines
  - ✓ Can be implemented Key pad scanner

❑ Supply
- 1.2V for digital core
- 2.5V for RF, analog IPs
- 3.3V for digital I/O

❑ Embedded Memory
- 1Mbit(internal)

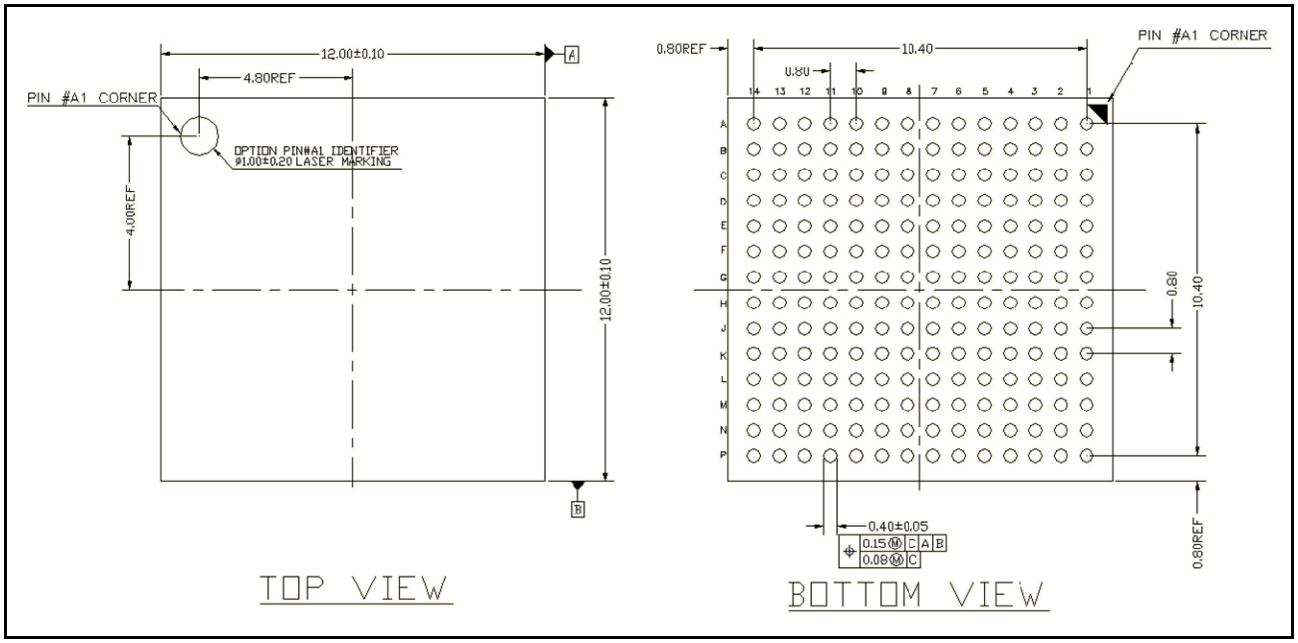
❑ Package
- FC3860A: 12x12 BGA, 196 pins, 0.8pitch

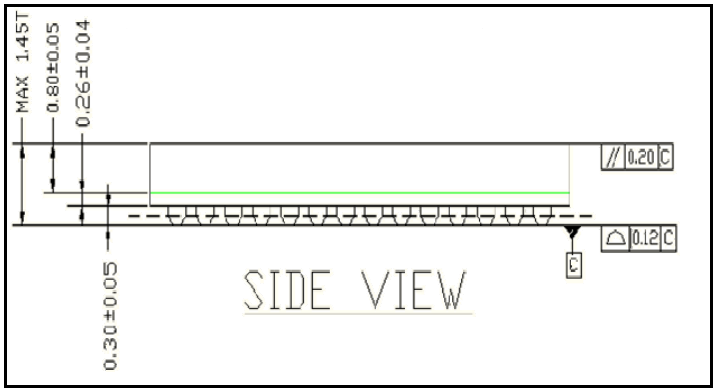
1.3. Block Diagram



[Figure 2 FC3860A Block Diagram]

2. Package Outline





[Figure 3 Package outline of FC3860A]